REMARKS

The claims are claims 1 to 4.

Claim 1 is amended to add subject matter illustrated in Figure 5 and described in the application at page 11, lines 1 to 7.

Claims 1 to 4 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Frankel et al U.S. Patent 4,463,443 and Kuboki et al U.S. Patent 5,058,114.

Claims 1 recites subject matter not made obvious by the combination of Frankel et al and Kuboki et al. Claim 1 recites a copy/access controller includes a counter and a comparator. These limitations are not made obvious by the combination of Frankel et al and Kuboki et al. The OFFICE ACTION cites: input data register 10 of Frankel et al as making obvious the claimed first buffer; output data register 14 of Frankel et al as making obvious the recited second buffer; and the elements RAM 16, RAM address counters 16a, RAM input holding register 18, RAM output holding register 20 and write and read sequence generator and control logic of Frankel et al as making obvious the recite copy/access controller. Presumably the recited first component is the apparatus supplying data to input data register 10 and the recited second component is the apparatus receiving data form output data register 14. The OFFICE ACTION states at page 2, line 24 to page 3, line 1:

> "Frankel does not teach the prompting of a second component to access the second buffer when the data is copied from the first buffer."

The Applicant agrees with this statement of the Examiner. Frankel et at states at column 3, lines 59 to 63:

> "In a similar manner, the data is output from the buffer at the output data register 14 synchronously with the output data clock. When the output data register 14 is empty, data in the RAM output register 20 is transferred to it."

This portion of Frankel et al teaches continuous output of data from output data register 14 to the second component not shown. This portion of Frankel et al fails to teach prompting this second component "when said count equals said buffer size" as recited in claim 1. Instead, this language strongly implies that access by the second component to data stored in the second buffer does not require any such prompting. The Applicant submits that the above quoted language of claim 1 requires more than merely writing to the output shift register. This language requires generation of a prompt signal by the copy/access controller to initiate reading data by the second component "when said count equals said buffer size." The Applicant submits this limitation is not inherent in the mere writing of data to the buffer. The OFFICE ACTION cites element 1 and column 4, lines 3 to 9 of the secondary reference Kuboki et al as making obvious this the previously recited version of the copy/access controller. Kuboki et al states at column 4, lines 3 to 9:

> "A state change bit SCB contained in the control register REG 4 is set by the core processor CPC 1 when a state transition occurs, sending an interrupt signal IRQ to the host processor HPC 14, prompting it to access and read the FIFO memory 15. The host processor HPC14 enables the state trace function mode by setting the state trace bit STB in the control register REG 4."

This teaching of Kuboki et al differs from the above quoted language of claim 1 because it makes obvious neither the recited counter nor the recited comparator. The Applicant respectfully submits that neither Frankel et al nor Kuboki et al teach the recited copy/access controller. Particularly, neither Frankel et

al nor Kuboki et al teach the recited copy/access controller includes the recited counter and the recited comparator. Accordingly, claim 1 is allowable over the combination of Frankel et al and Kuboki et al.

Claims 2 to 4 are allowable by dependence upon respective allowable base claim 1.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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